

CLAIMS

What is claimed is:

1. A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in a polysilicon gate electrode etching process comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

patterning the hardmask layer for forming a gate electrode according to a photolithographic patterning process;

carrying out a first reaction ion etch (RIE) step to etch through a thickness of the hardmask layer to expose the polysilicon layer;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power;

carrying out a third RIE step to etch through a second thickness portion of the polysilicon layer including at least one of a lower RF source power and RF bias power compared to the second RIE step;

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plasma treating the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert source gas to neutralize an electrical charge imbalance; and,

carrying out a fourth RIE etch process to etch through a remaining thickness of the polysilicon layer.

2. The method of claim 1, wherein the step of plasma treating is carried out using zero RF bias power.

3. The method of claim 1, wherein the fourth RIE process is carried out using zero RF bias power.

4. The method of claim 1, wherein the polysilicon layer includes an n-dope region and a p-doped region for forming respectively doped polysilicon gate electrodes in parallel.

5. The method of claim 1, wherein the RF source power and RF bias power are reduced in the third RIE Step.

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6. The method of claim 1, wherein the inert gas source is selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

7. The method of claim 1, wherein the fourth RIE etch is carried out with a chlorine-free etching chemistry.

8. The method of claim 7, wherein the chlorine-free etching chemistry comprises HBr and oxygen.

9. The method of claim 1, wherein the second and third RIE etch steps have an etching chemistry comprising the combination of one of HBr/Cl₂/O₂ and CF₄/Cl₂/O₂.

10. The method of claim 1, wherein the RF bias power is supplied at a frequency of greater than about 1 MHz adjustably decoupled from the RF source power.

11. The method of claim 1, wherein the gate dielectric is selected from the group consisting of thermally grown SiO₂ and binary oxides having a dielectric constant of greater than about 20.

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12. The method of claim 1, wherein the hardmask layer is selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

13. The method of claim 1, wherein the third RIE etch step is carried out with zero RF bias power applied.

14. A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in parallel etching of n and p-doped polysilicon gate electrodes comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer including n-doped and p-doped regions formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

patterning the hardmask layer according to a photolithographic patterning process for forming a polysilicon gate electrode;

carrying out a first reaction ion etch (RIE) step to etch through a thickness of the hardmask layer to expose the polysilicon layer;

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carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power.

carrying out a third RIE step to etch through a second thickness portion of the polysilicon layer including at least one of a lower RF source power and RF bias power compared to the second RIE step to expose a portion of the gate dielectric;

plasma treating in-situ with an inert gas plasma the exposed gate dielectric and polysilicon layer using a zero RF bias power to neutralize an electrical charge imbalance on the polysilicon gate electrode; and,

carrying out a fourth RIE etch process to etch through a remaining thickness of the polysilicon layer using a zero RF bias power.

15. The method of claim 14, wherein the RF source power and RF bias power are reduced in the third RIE Step.

16. The method of claim 14, wherein the inert gas source is selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

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17. The method of claim 14, wherein the fourth RIE etch is carried out with a chlorine-free etching chemistry.

18. The method of claim 17, wherein the chlorine-free etching chemistry comprises HBr and oxygen.

19. The method of claim 14, wherein the second and third RIE etch steps have an etching chemistry comprising the combination of one of HBr/Cl₂/O₂ and CF₄/Cl₂/O₂.

20. The method of claim 14, wherein the RF bias power is supplied at a frequency of greater than about 1 MHz adjustably decoupled from the RF source power.

21. The method of claim 14, wherein the gate dielectric is selected from the group consisting of thermally grown SiO₂ and binary lanthanum oxides having a dielectric constant of greater than about 20.

22. The method of claim 14, wherein the hardmask layer is selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

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23. The method of claim 14, wherein the second RIE etch step is carried out with zero RF bias power applied.